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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,116	08/29/2001	William R. Wheeler	10559/601001/P12885	6930

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EXAMINER	
FERRIS III, FRED O	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/942,116	WHEELER ET AL.	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-8 and 10-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-8 and 10-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been presented for examination based on applicant's amendment filed on 7 March 2005. Applicants have cancelled claims 4 and 9. Claims 1-3, 5-8, and 10-24 are currently pending in this application and remain rejected by the examiner.

Response to Arguments

2. Applicant's arguments filed 7 March 2005 have been fully considered.

Regarding applicant's response to the objection to the specification: The examiner withdraws the objection to the specification in view of applicant's amendment to the specification and supporting arguments filed 7 March 2005.

Regarding applicant's response to 112(1) rejection: The examiner withdraws the 112(1) rejection in view of applicant's amendment to the claims and arguments filed 7 March 2005. However, the examiner has now applied 35 USC 101 rejections to amended claims 1-3, and 5. (Please see 101 rejections below)

Regarding applicant's response to 102(b) rejections: The examiner withdraws the previous 102(b) rejection of in view of applicant's amendment to the claims.

Regarding applicant's response to 103(a) rejections: The examiner withdraws the previous prior art rejection of claims 1-3, 5-8, and 10-21 in view of applicant's amendment to the claims. However, claims 1-3, 5-8, and 10-21 now stand rejected under 103(a) based on new grounds for rejection (See new prior art rejections below).

Applicant's arguments regarding claims 22-24 have been fully considered but they are not persuasive. Specifically, applicants argue that Wang fails to teach copying the instruction to a second page and executing the second page starting with the instruction. The examiner asserts that this feature is necessarily obvious in view of Wang because Wang teaches copying to computer executable instructions (abstract) into secondary pages (CL1-L55-CL2-L7, Figs. 5-7) as part of the write protecting process. Hence a skilled artisan having access to the teachings of Wang would have known to execute the stored instructions from the second memory page out of necessity as part of the write protection process using the reasoning previously cited below under 103(a) rejections.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1-3, and 5 are rejected under 35 U.S.C. 101 because the claimed invention is drawn to non-statutory subject matter.

The Examiner submits that method claims 1-3, and 5 as written, are merely drawn to a mental process for simulating a logic design, since the language of the claims can be interpreted as meaning the method is carried out by a mental process

augmented (calculated) using pencil and paper. (i.e. not a computer process, such as via a hand written K-map or state table)

MPEP 2111 [R-1] recites the following:

"2111 [R-1] Claim Interpretation; Broadest Reasonable Interpretation
CLAIMS MUST BE GIVEN THEIR BROADEST REASONABLE INTERPRETATION
During patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000).< Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969) (Claim 9 was directed to a process of analyzing data generated by mass spectrographic analysis of a gas. The process comprised selecting the data to be analyzed by subjecting the data to a mathematical manipulation. The examiner made rejections under ***35 U.S.C. 101*** *and 102. In the 35 U.S.C. 102 rejection, the examiner explained that* ***the claim was anticipated by a mental process augmented by pencil and paper markings***. ***The court agreed that the claim was not limited to using a machine to carry out the process since the claim did not explicitly set forth the machine***. *The court explained that "reading a claim in light of the specification, to thereby interpret limitations explicitly recited in the claim, is a quite different thing from reading limitations of the specification into a claim,' to thereby narrow the scope of the claim by implicitly adding disclosed limitations which have no express basis in the claim." The court found that applicant was advocating the latter, i.e., the impermissible importation of subject matter from the specification into the claim.). See also In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997) (The court held that the PTO is not required, in the course of prosecution, to interpret claims in applications in the same manner as a court would interpret claims in an infringement suit. Rather, the "PTO applies to verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in applicant's specification.")"*

The Examiner further submits that, in view of the language of the claims, Applicant's have merely claimed a manipulation of abstract ideas by a mental process. Section 2106 [R-2] (Patentable Subject Matter — Computer-Related Inventions) of the MPEP recites the following:

"In practical terms, claims define nonstatutory processes if they:
– consist solely of mathematical operations without some claimed practical application (i.e., executing a "mathematical algorithm"); or
*– **simply manipulate abstract ideas**, e.g., a bid (Schrader, 22 F.3d at 293-94, 30 USPQ2d at 1458-59) or a bubble hierarchy (Warmerdam, 33 F.3d at 1360, 31 USPQ2d at 1759), **without some claimed practical application**."*

In this case, claims 1-3, and 5 are simply drawn to the manipulation of abstract ideas by the mental process of simulating a logic design by a process that is augmented (calculated) using pencil and paper. (i.e. not a computer process, such as via a hand written K-map or state table). The examiner suggests that amending the preamble of independent claim 1 to read "A computerized method of simulating logic design.." would render the claims statutory since it would explicitly set forth a machine process by computer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-3, 5-8, and 10-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,044,211 issued to Jain in view of U.S. Patent 5,819,072 issued to Bushard et al.

Independent claims 1, 6 and 11 are drawn to:

Method, article, and apparatus for simulating a logic design by:
storing first state to identify node in simulation with logic high value;
storing second state to identify node in simulation with logic low value;
storing third state to identify node in simulation with undefined state;
performing a three state simulation to determine an output of node in simulation based on first state, second state, and third state;
determining if simulation was successful based on whether output node has undefined state;
performing four state simulation of logic design if three state simulation was successful.

Regarding independent claims 1, 6, and 11: Jain discloses the simulation of a logic design (Figs. 4-6) inclusive of identifying and storing the state(s) of the node (CL13-L16-21, CL24-L17-26) and determining the output of the node (CL5-L55-59, CL24-L29) during simulation based on value(s) of the prior state(s) (CL21-L29-33, 50, 61-63). Hence, Jain renders obvious the elements of the limitations relating to storing and identifying multiple node states (i.e. first, second, third, etc.) based on a logic value. (Tabs. II-IV, Fig. 5)

Jain does not explicitly disclose four distinct state values (i.e. high, low, high impedance, and undefined).

Bushard teaches a four state simulator where the possible values include high (1), low (0), high impedance (unknown), and undefined (don't care). (CL9-L31-37, 57-

65, Figs. 7, 8) Determining if the simulation was successful based on the state of the output node is obvious in view of Bushard because Bushard teaches a four state simulation that identifies and stores the state values, and then subsequently analyzes the circuit design based these values (CL10-L3-15, i.e. high, low, unknown, etc.). Hence a skilled artisan having access to the teachings of Bushard would have known to use state values (i.e. four states, high, low, high impedance, and undefined, in determining if the simulation of the logic was successful.

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Jain relating to simulation of a logic design and identifying and storing node state values, with the teachings of Bushard relating to the use of multi-state values in logic design simulation, to realize the claimed invention. An obvious motivation exists since, in this case, the Jain reference teaches to the Bushard reference, and the Bushard reference teaches to the Jain reference. Specifically, both Jain and Bushard teach simulation of a logic designs and are used in the same technical arena as noted above. Jain teaches to Bushard because Jain discloses that node values can be detected and stored for a given state. (See: Jain, CL13-L16-21). Bushard teaches to Jain because Bushard specifically discloses using multi-state values in logic design simulation. (See: Bushard, CL9-L27-67, Figs. 7, 8) Further, the level of skill required by an artisan to realize the claimed limitations of the present invention is clearly established by both references. (See: Jain/Bushard, Abstracts) Accordingly, a skilled artisan having access to the teachings of Jain and Bushard, would have knowingly modified the teachings of Jain with the teachings of

Bushard (or visa versa) to realize the claimed elements of the present invention and gain the advantage of reduced development time and cost.

Per dependent claims 2, 7, and 12: Jain discloses determining node value based on value(s) of prior state(s) (CL21-L29-33, 50, 61-63), Bushard discloses determining four state logic simulation and hence would have been knowingly incorporated using the reasoning cited above.

Per dependent claims 3, 8, and 13: This limitation would obviously be required out of necessity since the third state represents an undefined state. That is, if two sources are driving the node, then obviously the state of the node is undefined since the value at the node will be somewhere in between the value of the first driving source, and second driving source. (i.e. the output of the node is therefore ambiguous) This feature is also disclosed by Bushard as previously noted above. (CL9-L27-67, Figs. 7, 8)

Per dependent claim 14: Bushard discloses fourth states in the logic design simulation and would have knowingly been incorporated using the reasoning previously cited above.

Per dependent claims 5, 10, and 15: Jain discloses determining the node output values based on selected values (high/low) of previous states as noted above. (CL5-L35-63)

Per independent claim 16: This claim merely requires storing three bits of state information, and then subsequently checking the three bits in simulating operation of the logic design. This claim is rendered obvious by the combination of Jain and Bushard

using the reasoning previously cited above. The examiner further notes that storing the state information as three bits representing to possible node states merely amounts to bit pattern mapping of the state values and hence would have been knowingly implemented by a skilled artisan (see: bit map/pattern, Microsoft Computer Dictionary, Third Edition, 1997).

Per dependent claims 17-21: Bushard discloses determining the stored state/node value (high, low, etc.) based on up to four bits (CL9-L27-67, Figs. 7, 8) and considers undermined states and high impedance states and hence would have been knowingly implemented by a skilled artisan using the reasoning cited above.

5. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,466,898 issued to Chan in view of U.S. Patent 6,738,875 issued to Wang.

Per independent claim 22: Chan teaches a cycle-based simulation (CL1-L45-57, CL2-L5-21, Figs. 3, 8, 11) of a logic design inclusive of logic computation instructions (CL4-L5-19, Tab. 1) and multiple memory pages (CL8-L13-24).

Chan does not explicitly disclose a write-protected memory.

Wang teaches techniques for write protecting a memory page, copying to secondary pages, un-protecting a write-protected page, rewriting values, and re-protecting the original write protected page. (CL1-L55-CL2-L7, Figs. 5-7)

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Chan relating to a cycle-based

simulation, with the teachings of Wang relating to write protecting memory pages, to realize the claimed invention. An obvious motivation exists since this area of technology is highly competitive with many cycle-based simulation tools available in the market place and large amounts of money being spent in product development and improvement. (See: Wang, Table 1, for example) Accordingly, a skilled artisan would have made an effort to become aware of what capabilities had already been developed in the market place and, hence, would have knowingly modified the teachings of Chan with the teachings of Wang in order to reduce development time and cost.

Per dependent claims 23-24: These claims merely require inserting an illegal instruction into the memory page to trigger an exception to the write protection process. This technique is well known in the art and would have knowingly been used by a skilled artisan as a method of generating a processor interrupt for handling write protection routine. (See: definition for "exception", Microsoft Computer Dictionary", Third Edition, 1997)

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 6,718,522 issued to Mc Bride et al teaches simulating logic design and storing node state values.

"Process-Level Modeling with VHDL", J. Armstrong, Proceeding Verilog HDL Conference, March 1998, IEEE teaches simulating logic design and storing node state values.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: (703) 872-9306

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